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EXAMINER	
PATEL, PARESH H	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,581	SU ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *21 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Corr (GB 2 332 775 A).

Regarding claim 1, Corr in fig. 1-3 discloses a method of electrically and optically testing [see Abstract] a planar lightwave circuit [electronic/optical integrated circuit die, also see lines 4-5 on page 1] comprising:

placing the planar lightwave circuit [electronic/optical integrated circuit die 12] on a test fixture [fig. 3], the test fixture including a printed circuit board [where 26 is mounted];

electrically coupling the printed circuit board to the planar lightwave circuit [using 26];

electrically coupling the printed circuit board to a tester [32 and lines 27-28 of page 2];

optically coupling [using 28 and 16] the planar lightwave circuit to the tester; and

performing electrical and optical testing of performance of the planar lightwave circuit [lines 27-28 of page 2].

3. Claim 1 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Allie et al. (US 5400417).

Regarding claim 1, Allie et al. (hereafter Allie) in fig. 2 discloses a method of electrically and optically testing [see Abstract] a planar lightwave circuit comprising:

placing the planar lightwave circuit [16, 18, 20, 22, 24, 26] on a test fixture [10], the test fixture including a printed circuit board [pcb of 14];

electrically coupling [using 30 or 28] the printed circuit board to the planar lightwave circuit;

electrically coupling the printed circuit board to a tester [50, 46, 42];

optically coupling [using 36] the planar lightwave circuit to the tester; and

performing electrical and optical testing of performance of the planar lightwave circuit [to null the bias control error to zero, see lines 1-4 of column 3].

4. Claims 1-2 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Spaziani et al. (US 5631571).

Regarding claim 1, Spaziani et al. in fig.

a method of electrically and optically testing a planar lightwave circuit comprising:

placing the planar lightwave circuit [218 of 100] on a test fixture [308], the test fixture including a printed circuit board [308];

electrically coupling [via 116, see fig. 3] the printed circuit board to the planar lightwave circuit;

electrically coupling [via 308, see fig. 3] the printed circuit board to a tester;

optically coupling [via 114, see fig. 3] the planar lightwave circuit to the tester; and

performing electrical and optical testing of performance of the planar lightwave circuit [see fig. 3].

Regarding claim 2, Spaziani discloses a vacuum [vacuum chuck 200] as claimed.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1, 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sjölinder et al. (US 5715338) in view of Corr (GB 2 332 775 A).

Regarding claim 1, Sjölinder et al. (hereafter Sjölinder) discloses a method of electrically and optically testing a planar lightwave circuit comprising:

placing the planar lightwave circuit [11] on a test fixture [3], the test fixture including a printed circuit board [3];

electrically coupling [via 13] the printed circuit board to the planar lightwave circuit;

electrically coupling [via 18'] the printed circuit board to a tester;

optically coupling [via 9] the planar lightwave circuit to the tester; and

performing electrical and optical testing of performance of the planar lightwave circuit.

Sjölinder discloses all the elements except for a tester and performing electrical and optical testing of performance of the planar lightwave circuit.

Corr discloses a tester [fig. 3] to perform electrical and optical testing of the planar lightwave circuit [12]. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use tester of Corr for planar lightwave circuit of Sjölinder, in order to enable function testing prior to packaging.

Regarding claims 3-7, Sjölinder in fig. 1 discloses all the claimed elements including solder wires 13, an electrical connector 16 and conductive epoxy 13 as claimed.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corr as applied to claim 1 above, and further in view of Spaziani et al. (US 5631571).

Regarding claim 1, Corr discloses all the elements except for holding the planar lightwave circuit in place using a vacuum. However, Corr discloses a chuck 24 to hold the die 12 during testing. Spaziani et al. (hereafter Spaziani) in fig. 1-2 discloses holding the planar lightwave circuit [218 of 100] in place using a vacuum [200]. Spaziani also discloses testing of wafer that includes semiconductor device 218, which has optical port 203. It would have been obvious to a person having ordinary skill in the art at the

time the invention was made to modify chuck of Corr with vacuum chuck of Spaziani, in order to hold the wafer during testing.

8. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corr as applied to claims 1 above, and further in view of Forsyth et al. (US 4910548).

Regarding claims 3 and 5, Corr discloses all the elements except for soldering wires from the printed circuit board to the planar light wave circuit. Forsyth discloses soldering wires (wire bonding for claim 5) [55 or 52] from the printed circuit board [40] to the planar light wave circuit [30]. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use soldering wires (which is known in the art) as taught by Forsyth, in order to obtain electrical connection between printed circuit board and planar light wave during testing.

Regarding claims 4 and 6, Forsyth in fig. 7 and 9 discloses attaching an electrical connector [92, 93] to the printed circuit board, the electrical connector coupled to the tester via a ribbon cable [112 and 111 and lines 43-62 of column 7].

Regarding claim 7, Corr discloses all the elements except for using a conductive epoxy and wires to electrically couple the printed circuit board to the planar light wave circuit. Forsyth discloses gold wires [52, 55]. It would have been an obvious matter of design choice to use a conductive epoxy and wires to electrically couple the printed circuit board to the planar light wave circuit, since applicant has not disclosed that use of conductive epoxy and wires as claimed solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with

combination of Corr and Forsyth to electrically couple the printed circuit board to the planar light wave circuit during testing.

9. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spaziani as applied to claims 1 above, and further in view of Forsyth et al. (US 4910548).

Regarding claims 3 and 5, Spaziani discloses all the elements except for soldering wires from the printed circuit board to the planar light wave circuit. Forsyth discloses soldering wires (wire bonding for claim 5) [55 or 52] from the printed circuit board [40] to the planar light wave circuit [30]. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use soldering wires (which is known in the art) as taught by Forsyth, in order to obtain electrical connection between printed circuit board and planar light wave during testing.

Regarding claims 4 and 6, Forsyth in fig. 7 and 9 discloses attaching an electrical connector [92, 93] to the printed circuit board, the electrical connector coupled to the tester via a ribbon cable [112 and 111 and lines 43-62 of column 7].

Regarding claim 7, Spaziani discloses all the elements except for using a conductive epoxy and wires to electrically couple the printed circuit board to the planar light wave circuit. Forsyth discloses gold wires [52, 55]. It would have been an obvious matter of design choice to use a conductive epoxy and wires to electrically couple the printed circuit board to the planar light wave circuit, since applicant has not disclosed that use of conductive epoxy and wires as claimed solves any stated problem or is for

any particular purpose and it appears that the invention would perform equally well with combination of Spaziani and Forsyth to electrically couple the printed circuit board to the planar light wave circuit during testing.

Response to Arguments

10. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 571-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 31, 2006

Paresh Patel 01/31/06
Primary Examiner
AU 2829